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APPLICATION NO	Э.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/071,795	•	02/06/2002	Raul-Adrian Cernea	M-10314 US	2871
3625.7	7590	01/09/2004		EXAMINER	
		& DE RUNTZ LLP Y STREET	NGUYEN, TH	NGUYEN, THAN VINH	
SUITE 18		I SIKEEI	ART UNIT	PAPER NUMBER	
SAN FRA	NCISCO,	CA 94111	2187	12	
				DATE MAILED: 01/09/2004	10

Please find below and/or attached an Office communication concerning this application or proceeding.

Application No. Application State Art Unit Than Nguyen 2187 Art Unit 21									
## Examiner Than Nguyen 2187 218		Application No.	Applicant(s)						
Than Nguyen - The MALLING DATE of this communication appears on the cover sheet with the correspondence address → Period for Reply A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ③ MONTH(S) FROM THE MALLING DATE OF THIS COMMUNICATION. Estentions of term may be available under the proximate of J CFR 1.13(ii), in no event, however, may a reply be limely flied Estentions of many by a semilate under the proximate of J CFR 1.13(iii), in no event, however, may a reply be limely flied Estentions of many by a semilate under the proximate of J CFR 1.13(iii), in no event, however, may a reply be limely flied If the period for may by specified show is less than thisy (80) cays, a may within his stationy minimum of thiny (80) days will be considered timely. If the period for may be specified with the man thiny (80) cays, a many within his station, and the station of the period of the communication. If the period for may is specified with the proximate of the manifest and the station is reply than the station of the manifest and the station is reply than the station of the manifest and the station is reply than the station is non-final. 3) □ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11, 453 O.G. 213. Disposition of Claims 4) □ Claim(s) is/are pending in the application. 4a) Of the above claim(s) is/are withdrawn from consideration. 5) □ Claim(s) is/are objected to by the Examiner. 10) □ The specification is objected to by the Examiner. 10) □ The specification is objected to by the Examiner. 20) □ The specification is objected to by the Examiner. 21) □ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). 21) □ The cath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152. Priority under 35 U.S.C. §§ 119 and 120 12) □ Acknowledgment is made of a claim for for	Office Action Summany	10/071,795	CERNEA, RAUL-ADRIAN						
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DETAILED ACTION

- 1. This is a response to the amendment and IDS, filed 8/1/03 and 9/2/03.
- 2. Claims 1-38 are pending.
- 3. In response to the amendment to the title, the previous objection to the title is withdrawn.
- 4. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection. Based on new discovered prior arts, the previous indication of allowance is withdrawn.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 6. Claim 1-38 is rejected under 35 U.S.C. 102(b) as being anticipated by Estakhri et al (USP 5,907,856).

As to claim 1,11,29:

7. Estakhri teaches a device for storing mapping information. Estakhri teaches the claimed non-volatile memory system comprising: a controller for externally transferring data identified by logical sector addresses (controller 532; Fig. 10); and a memory connected to the controller, ((memory; 3/55-65, 4/20-24) comprising: an array comprised of a plurality of sectors, wherein

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each sector contains a plurality of data storage elements and is identified by a physical address; and a pointer structure storing correspondences between logical sector addresses and physical sector addresses, wherein the pointer structure concurrently maintains a first correspondence between a logical sector address and a first physical sector address at which currently valid data identified by the logical sector address is stored and a second correspondence between the logical sector address and a second distinct physical sector address at which previously valid data identified by the logical sector address has been stored (4/34-50, 11/64-12/20).

As to claim 2,12,33:

8. Estakhri teaches correspondences are stored in non-volatile storage elements of the pointer structure (6/22-25).

As to claim 3,14:

9. Estakhri teaches read and write circuitry coupled to the array and the pointer structure, wherein the array and the pointer structure have distinct decoder structures (flash controller 532; 10/15-17).

As to claim 4,13:

10. Estakhri teaches the correspondences are stored in binary non-volatile storage elements and the data storage elements are multi-state (12/50-13/5).

As to claim 5:

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11. Estakhri teaches the controller and said memory are formed on separate integrated circuits

(Fig. 10).

As to claim 6,15,30:

12. Estakhri teaches the memory concurrently maintains the currently valid data identified by the logical sector address and the previously valid data identified by the logical sector address

(11/64-12/20).

As to claim 7,19,34,35:

13. Estakhri teaches the controller can access the previously valid data identified by the logical

sector address in response to a command (9/34-50; 11/64-12/20).

As to claim 8,16:

14. Estakhri teaches said memory comprising: write circuitry coupled to the memory array and

the pointer structure, wherein during a write process new data corresponding to a specified

logical sector address is written into the array at a new physical sector address of the array

concurrently with a new correspondence between the specified logical sector address and the new

physical sector address being stored in the pointer structure (11/64-12/20).

As to claim 9,17,31,32:

15. Estakhri teaches said memory further comprising: erase circuitry coupled to the array

whereby said previously valid data is erasable in a background erase process (6/3-21).

As to claim 10,18:

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16. Estakhri teaches each sector of the array has an associated flag bit, the integrated circuit further comprising: a determination circuit connected to the write circuitry and the array, whereby an available sector is determined for the new physical sector address based on the associated flag bits (7/1-8/12)

As to claim 20,21,38:

17. Estakhri teaches a method of operating a memory system comprising a controller and a memory, the memory including a pointer structure and an array comprised of a plurality of sectors, wherein each sector is identified by a physical address and contains a plurality of non-volatile data storage elements, the method comprising: receiving at the controller unit from a host a first data set and a logical sector address whereby the host identifies the first data set; transferring the first data set and the logical sector address from the controller to the memory; storing the first data set at a first physical sector address of the array; storing a first correspondence between the logical sector address and the first physical sector address in the pointer structure; subsequent to said storing the first data set and said storing the first correspondence, receiving at the controller from the host a second data set to be stored at the logical sector address; transferring the second data set from the controller to the memory; storing the second data set at a second physical sector address of the array; and storing a second correspondence between the logical sector address and the second physical sector address in the pointer structure, wherein the memory retains the first data set at the first physical sector address

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and the first correspondence in the pointer structure subsequent to said storing the second data set and said storing the second correspondence (Fig 4; 7/7-8/12, 11/64-12/20).

As to claim 22:

18. Estakhri teaches storing the second data set and the second correspondence, erasing the first physical sector (6/3-21).

As to claim 23:

19. Estakhri teaches erasing is performed in a background process (6/3-21).

As to claim 24:

20. Estakhri teaches the pointer structure is non-volatile (6/22-25).

As to claim 25,26:

21. Estakhri teaches storing the second data set and the second correspondence, receiving at the controller a request from the host for data stored at the logical sector address; providing the request from the controller to the memory in terms of the logical sector address; and providing the second data set from the memory to the controller in response to the memory receiving the request in terms of the logical sector address (4/34-50, 11/64-12/20).

As to claim 27,36:

22. Estakhri teaches prior to said storing the first data set, selecting the first physical sector address from a set of available sector addresses; and prior to said storing the second data set, selecting the second physical sector address from the set of available sector addresses (7/6-8/13).

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As to claim 28,37:

23. Estakhri teaches said set of available sector addresses corresponds to only good physical

sectors (good available space; 7/40-47).

Conclusion

24. Any inquiry concerning this communication or earlier communications from the examiner

should be directed to Than Nguyen whose telephone number is (703) 305-3866. The examiner

can normally be reached on M-F from 8:00 a.m. to 3:00 p.m. EST.

25. Any inquiry of a general nature or relating to the status of this application should be

directed to the Group receptionist whose telephone number is (703) 305-9600.

26. The fax phone number for Art Unit 2187 is 703-308-9051 or 703-308-9052.

Than Nguyen

Primary Patent Examiner

December 31, 2003

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